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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,144	02/23/2004	Woon-bae Kim	277/036	5370
7590	04/06/2005		EXAMINER	
LEE & STERBA, P.C. Suite 2000 1101 Wilson Boulevard Arlington, VA 22209			NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)
	10/784,144	KIM ET AL.
	Examiner	Art Unit
	Khiem D. Nguyen	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 04 February 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 23 February 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

The non-final rejection as set forth in paper No. (103104) mailed November 4th, 2004 is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action. Claims (1-20) are pending in the application.

Claim Rejections - 35 USC § 103

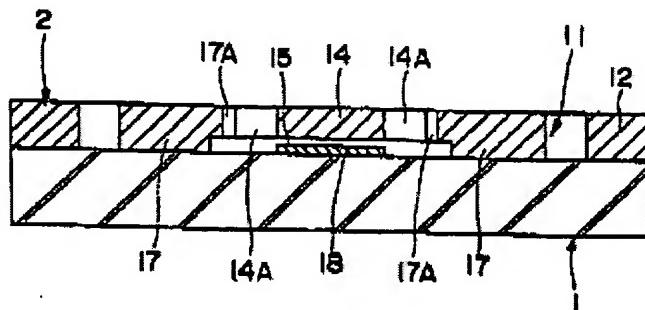
The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent 6,300,676) in view of Koopmans (U.S. Pub. 2004/0035917).

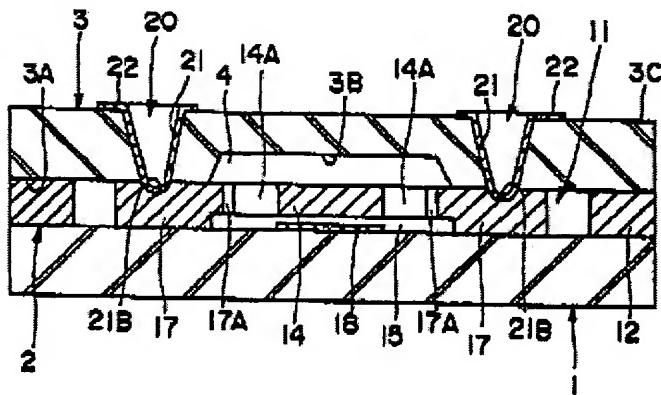
In re claim 1, Kawai discloses a method for manufacturing micro electro-mechanical systems, comprising: (a) forming an insulation layer on an upper surface of a semiconductor substrate **1** and patterning the insulation layer; (b) forming a structure layer **2** on an upper surface of the patterned insulation layer and etching the structure layer **2** (col. 9, lines 3-9 and FIG. 6);

FIG. 6



(c) forming an under bump metal 22 on a predetermined position of an upper surface of the structure layer 2; (d) forming a via hole 21 in a glass substrate 3 corresponding to the position of the under bump metal 22 of the structure layer and in a shape such that the via hole 21 is larger in diameter at an upper surface 21A of the glass substrate than at a lower surface 21B of the glass substrate 3, wherein the glass substrate 3 is bonded to the upper surface 21A of the structure layer 2 and creates a vacuum chamber 4 that protects a structure of the structure layer 2 (col. 9, line 11 to col. 10, line 50 and FIGS. 7, 9, 10, and 12); and

FIG. 10



(e) arranging a solder ball 23 on the bump metal 22 and bonding the solder ball 23 to the under bump metal 22 (col. 10, lines 33-42).

Kawai does not explicitly disclose arranging a solder ball in the via hole and bonding the solder ball to the under bump metal by melting the solder ball as required by the Applicants' claimed invention.

Koopmans, however discloses forming via holes 132 in a glass substrate 130 corresponding to the position of the under bump metal 122 of the structure layer 121

wherein the glass substrate 130 is bonded to the upper surface of the structure layer 121; and arranging solder balls 240 in the via holes 132 and bonding the solder ball 240 to the under bump metal 122 by melting the solder ball 240 (page 2, paragraph [0022] to page 3, paragraph [0030] and FIG. 1B).

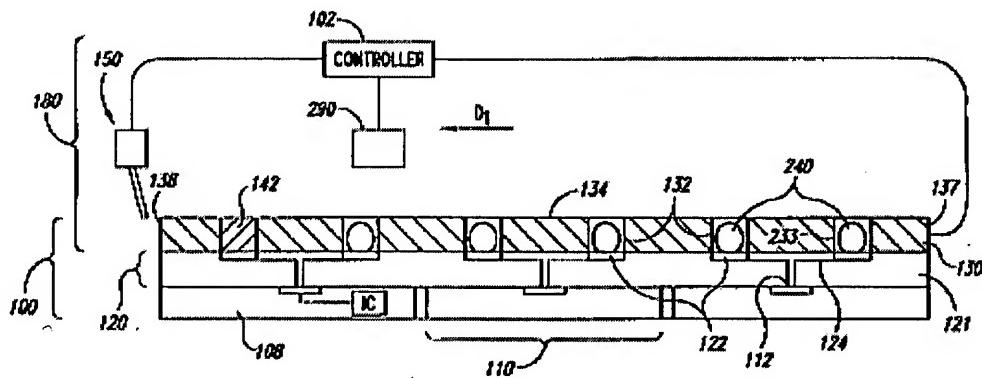


Fig. 1B

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Kawai and Koopmans to enable the process of arranging solder balls in the via holes and bonding the solder balls to the under bump metal by melting the solder balls of Kawai to be performed and furthermore to obtain systems having a fine pitch between the under bump metal (page 4, paragraph [0038], Koopmans).

In re claim 2, Kawai discloses wherein in (b), the structure layer is formed using an inductively coupled plasma-reaction ion etching (ICP-RIE) (col. 9, lines 3-9).

In re claim 3, Kawai discloses wherein in (d), the via hole 21 is formed using one selected from the group consisting of sand blasting, laser ablation and wet etching (col. 9, lines 23-43).

In re claim 4, Kawai discloses wherein in (d), the glass substrate **3** is bonded to the upper surface of the structure layer **2** using either anodic bonding or soldering (col. 9, lines 10-22).

In re claim 5, Kawai discloses wherein (d) further comprises removing an oxidation layer, which is bonded onto the upper surface of the structure layer (FIG. 8).

In re claim 6, Kawai discloses wherein the oxidation layer is removed either by printing a flux or by melting under an inert gas atmosphere without the flux (col. 9, lines 10-43).

In re claim 7, Kawai discloses wherein in (a), the semiconductor substrate **1** is a silicon substrate (col. 6, lines 57-60).

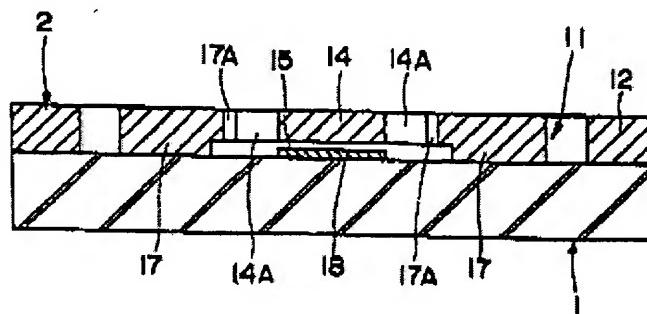
In re claim 8, Kawai discloses wherein in (b), the insulation layer is formed of one selected from the group consisting of Cr/Au alloy, Ti/Au alloy and Cr/Ni/Au alloy (col. 7, lines 16-64).

In re claim 9, Kawai discloses wherein in (c), the under bump metal **22** is formed of one selected from the group consisting of Cr/Au alloy, Ti/Au alloy, Cr/Ni/Au alloy and Cu/Ni/Au alloy (col. 9, lines 44-59).

In re claim 10, Kawai discloses wherein in (e), the solder ball **23** is formed of one selected from the group consisting of Sn/pb alloy, In/Sn alloy, Au/Sn alloy, Ag/Cu alloy, In/Ag alloy, In/Bi alloy, Sn/Bi alloy, Sn/Cu alloy, Ag/Sn alloy, Sn/Ag/Cu alloy, Sn/Ag/Cu/Bi alloy, Sn/Ag/Bi alloy and Sn/Zn alloy (col. 9, lines 44-59).

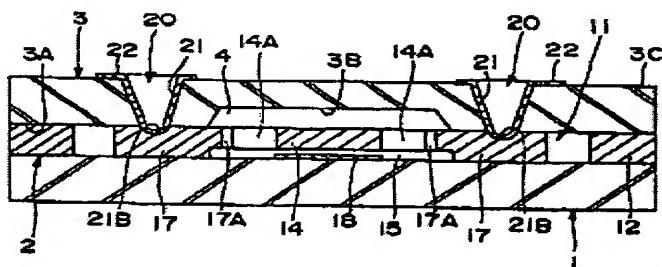
In re claim 11, Kawai discloses a method for manufacturing micro electro-mechanical systems, comprising: (a) forming an insulation layer on an upper surface of a

semiconductor substrate 1 and patterning the insulation layer; (b) forming a structure layer 2 on an upper surface of the patterned insulation layer and etching the structure layer 2 (col. 9, lines 3-9 and FIG. 6);

FIG. 6

(d) forming a via hole 21 in a predetermined position of a glass substrate 3 and in a shape such that the via hole 21 is larger in diameter at an upper portion 21A of the glass substrate than at a lower portion 21B of the glass substrate 3, wherein the glass substrate is bonded to the upper surface of the structure layer 2 and creates a vacuum chamber 4 that protects a structure of the structure layer 2;

(d) forming an under bump metal 22 in a bottom of the via hole 21 and forming via side metal on an inner wall of the via hole (col. 9, line 11 to col. 10, line 50 and FIGS. 7, 10, and 12); and

FIG. 10

(e) disposing a solder ball 23 on the under bump metal 22 and bonding the solder ball 23 to the under bump metal 22 and via side metal (col. 10, lines 33-42).

Kawai does not explicitly disclose disposing a solder ball in the via hole and bonding the solder ball with the under bump metal and the via side metal by melting the solder ball as required by the Applicants' claimed invention.

Koopmans, however discloses forming via holes 132 in a glass substrate 130 corresponding to the position of the under bump metal 122 of the structure layer 121 wherein the glass substrate 130 is bonded to the upper surface of the structure layer 121; and disposing solder balls 240 in the via holes 132 and bonding the solder ball 240 with the under bump metal 122 and the via side metal by melting the solder ball 240 (page 2, paragraph [0022] to page 3, paragraph [0030] and FIG. 1B).

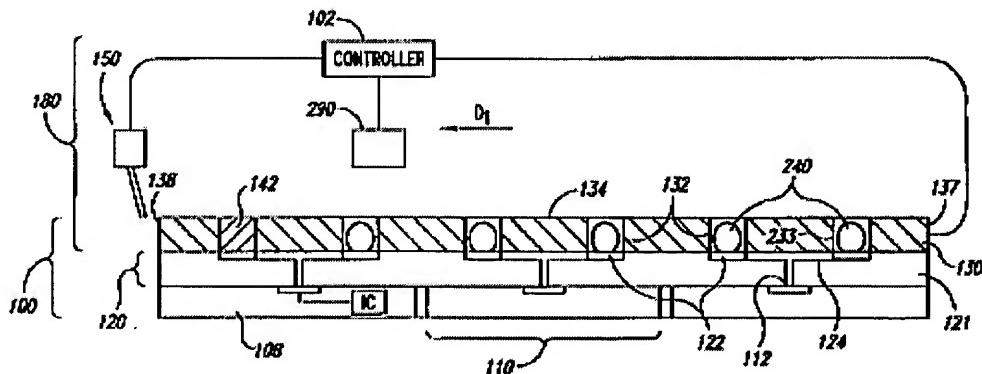


Fig. 1B

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Kawai and Koopmans to enable the process of disposing solder balls in the via holes and bonding the solder balls to the under bump metal and the via side metal by melting the solder balls of Kawai to be

performed and furthermore to obtain systems having a fine pitch between the under bump metal (page 4, paragraph [0038], Koopmans).

In re claim 12, Kawai discloses wherein in (b), the structure layer is formed using an inductively coupled plasma-reaction ion etching (ICP-RIE) (col. 9, lines 3-9).

In re claim 13, Kawai discloses wherein in (d), the via hole 21 is formed using one selected from the group consisting of sand blasting, laser ablation and wet etching (col. 9, lines 23-43).

In re claim 14, Kawai discloses wherein in (d), the glass substrate 3 is bonded to the upper surface of the structure layer 2 using either anodic bonding or soldering (col. 9, lines 10-22).

In re claim 15, Kawai discloses wherein (d) further comprises removing an oxidation layer, which is bonded onto the upper surface of the structure layer (FIG. 8).

In re claim 16, Kawai discloses wherein the oxidation layer is removed either by printing a flux or by melting under an inert gas atmosphere without the flux (col. 9, lines 10-43).

In re claim 17, Kawai discloses wherein in (a), the semiconductor substrate 1 is a silicon substrate (col. 6, lines 57-60).

In re claim 18, Kawai discloses wherein in (b), the insulation layer is formed of one selected from the group consisting of Cr/Au alloy, Ti/Au alloy and Cr/Ni/Au alloy (col. 7, lines 16-64).

In re claim 19, Kawai discloses wherein in (d), the under bump metal **22** and the via side metal are formed of one selected from the group consisting of Cr/Au alloy, Ti/Au alloy, Cr/Ni/Au alloy and Cu/Ni/Au alloy (col. 9, lines 44-59).

In re claim 20, Kawai discloses wherein in (e), the solder ball **23** is formed of one selected from the group consisting of Sn/pb alloy, In/Sn alloy, Au/Sn alloy, Ag/Cu alloy, In/Ag alloy, In/Bi alloy, Sn/Bi alloy, Sn/Cu alloy, Ag/Sn alloy, Sn/Ag/Cu alloy, Sn/Ag/Cu/Bi alloy, Sn/Ag/Bi alloy and Sn/Zn alloy (col. 9, lines 44-59).

Response to Applicants' Amendment and Arguments

Applicants contend that the Kawai reference (U.S. Patent 6,300,676) disclose a solder ball outside of a via hole and not a solder ball in the via hole, as recited in independent claims 1 and 11.

In response to Applicants' contention that Kawai does not teach or suggest arranging a solder ball in the via hole. Applicants' argument is moot since the newly discovered reference Koopmans (U.S. Pub. 2004/0035917) discloses forming via holes **132** in a glass substrate **130** corresponding to the position of the under bump metal **122** of the structure layer **121** wherein the glass substrate **130** is bonded to the upper surface of the structure layer **121**; and arranging solder balls **240** in the via holes **132** and bonding the solder ball **240** to the under bump metal **122** by melting the solder ball **240** (page 2, paragraph [0022] to page 3, paragraph [0030] and FIG. 1B). Thus, the newly discovered reference, Koopmans, in combination with the Kawai reference disclose the Applicants' claimed invention.

For these reasons, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
April 2nd, 2005



**W. DAVID COLEMAN
PRIMARY EXAMINER**